Nonlinear Analysis Tools for the Optimized Design of Harmonic-Injection Dividers

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***Abstract*—New nonlinear analysis tools for harmonic-injection dividers are presented based on bifurcation concepts. The advantage of these tools is their application simplicity and efficiency, which has enabled their use for actual circuit design and optimization. The tools allow control over the divided frequency and output power and predict the variation of the synchronization bands versus the circuit element values, which enables the design correction. They have been extended to the analysis and optimization of phase-locked harmonic-injection dividers, which contain a low-frequency feedback loop. The use of this loop, together with the accuracy of the analysis, has enabled the implementation of novel frequency-division functions, such as the division of variable order, versus a circuit parameter, or the division by fractional order. The output noise of the frequency dividers is analyzed through the conversion-matrix approach, studying the noise variation along the division bands. The new techniques have been applied to the design of a frequency divider by order 4 and 5, with 18-GHz input frequency, obtaining excellent agreement with the experimental results.**

***Index Terms*—Bifurcation, frequency divider, harmonic injection, optimization methods, phase locking, phase noise.**

I. Introduction

THE frequency divider is an essential component of modern communication systems. Digital dividers are commercially available up to Ku-band [1]. For higher input frequencies, analog dividers must be used, specifically designed for each project. When employing concepts from digital electronics, the number of transistors usually turns out to be extremely large. This increases the computation time and prevents the application of analysis techniques such as harmonic balance (HB) [2]. On the other hand, analog division based on harmonic-injection locking can be achieved with one or two transistors only. It has no limitation in the operating frequency, which can be as high as the maximum oscillation frequency of the transistors employed in the design. In addition, the reduced number of active devices should give smaller phase-noise values. However, the analog division is typically narrow-band [1]. The bandwidth decreases with the division order, so this order is generally limited to two or three.

In recent studies [3], techniques to increase the operation bandwidth of fundamentally synchronized oscillators have been proposed, with excellent experimental results. The techniques consist in the introduction of an external low-frequency feedback loop and the new circuit is called injection-locked phase-locked loop (ILPLL). Their application to harmonic-injection dividers is also possible, but requires an accurate prediction of the circuit behavior. In [3], the synchronization bandwidth is estimated through approximate expressions, but no nonlinear simulation, taking into account the entire harmonic content and accurate description of the circuit elements, is carried out. The difficulties in the design and simulation of harmonic-injection dividers are due to the complex subharmonic regime in which these circuits operate. Actually, the division bands are delimited by bifurcation phenomena [4]–[6] and exhaustive parametric simulations of microwave dividers have only been presented for division order $N = 2$ [2], [6]. Frequency division of higher order requires control over the self-oscillation and its harmonic content and the capability to correct the negative effects of parasitics and line discontinuities.

In this paper, new nonlinear analysis techniques for frequency dividers, based on accurate bifurcation detection, are presented. They have the advantage of their straightforward application to complex microwave circuits, not requiring the use of parameter-switching [2], [6] continuation methods, which has facilitated the extension to divisions by high order N. The application simplicity allows the employment of these techniques for actual circuit design and optimization. Today, and due to the high nonlinearity of the frequency-division regime, it is not possible to impose in advance the division bandwidth as a design specification. Instead, a new procedure is presented here, based on the determination of bifurcation loci versus the circuit-element values, using additional constraints over the free-running oscillation point. The increased control over the synchronized solution has enabled the investigation of new analog functions such as the switching of the division order between N and $N+1$ and the division by fractional order M/N.

In [3], it was shown how the introduction of a low-frequency loop into an injection-locked oscillator enabled the phase locking of the oscillator, giving rise to a substantial increase of the synchronization band. One of the novelties of the study carried out here is the introduction of this low-frequency loop to enlarge the inherently narrow division bands $1/N$ and M/N. The new design and simulation tools are applied to this frequency-divider configuration for an optimized design. The output noise of the dividers is analyzed, studying its variation along the division bands and the influence of the proximity to the band limits. To illustrate the new techniques, a MESFET-based divider, with 18-GHz input frequency, has been designed and made. The objective is the design of a harmonic-injection frequency divider by $N = 4$, in combination

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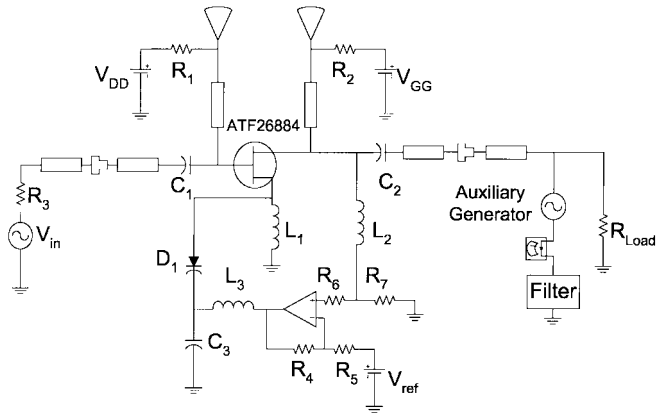

Fig. 1. Schematic of the harmonic-injection divider. The low-frequency feedback loop is included at a later design stage. This loop consists of a differential amplifier, with a reference dc signal, plus two RF chokes. The AG is used for analysis and optimization.

with phase-locking techniques, through the introduction of a low-frequency feedback loop. The input-frequency band for division by $N = 5$ is also determined, studying the possibility of switching the division order between these two values. The new techniques enable the optimization of the divider for an initially selected topology that is maintained through the whole design process. Here, a relatively simple topology has been employed, although the techniques can equally be applied to more complex circuits. It must be emphasized that the aim is not to present an ultimate divider topology, but to show the capabilities and flexibility of the new tools for an optimized design of harmonic-injection dividers, which constitute a valuable choice for narrow-band applications at high microwave frequencies.

This paper is organized as follows. Section II is devoted to the optimization of the free-running oscillator regime in which the harmonic-injection divider operates in the absence of input signal. The aim is to improve the frequency-division capabilities of the circuit once the input generator is connected. In Section III, techniques for the nonlinear analysis of the frequency divider by order N are presented. In Section IV, the design is optimized to correct the effect of parasitic elements. The low-frequency feedback loop is introduced at this stage. The fractional order division M/N is studied in Section V. The output noise of the frequency divider is analyzed in Section VI. The variations of both the phase and amplitude noise spectral densities along the frequency-division bands will be studied. In the Appendix, some concepts from nonlinear dynamics that directly apply to harmonic-injection frequency dividers are summarized.

II. Optimization of the Free-Running Oscillation

To obtain a harmonic-injection divider (see the Appendix), to which phase-locking techniques are to be applied, a voltage-controlled oscillator (VCO) must be initially designed. The topology chosen here (Fig. 1) uses source feedback (with the inclusion of a varactor diode) to achieve the free-running oscillation. Since the objective is the design of a frequency divider by $N = 4$, with 18-GHz input frequency, the oscillation frequency must be $f_o = 4.5$ GHz. A bias point $V_{\rm GS1}$, $V_{\rm DS1}$ is initially selected, fitting the gate circuit so as to obtain negative resistance at the drain terminal about the desired oscillation frequency f_o. To complete the oscillator design, a load circuit, enabling resonance at f_o, is introduced at the drain port. The circuit is analyzed through HB, with the aid of a voltage auxiliary generator (AG) [2], [4]. The AG is connected in parallel at a circuit node (Fig. 1) and allows the nonlinear optimization of the circuit for prefixed values of the steady-state oscillation frequency and amplitude. The AG frequency is set to the desired oscillation frequency ($f_{\rm AG} = f_o$) and its amplitude ($V_{\rm AG} = V_o$) can be fixed according to the desired voltage value at the AG location. Here, two different locations have been employed. At the transistor terminals, like the drain terminal, better sensitivity is obtained, so this location is useful at initial design stages. In parallel with the 50-Ω load, it enables the fixing of the output power. This power will, of course, have limitations inherent to the active devices and the circuit topology. In order for the voltage AG not to short circuit the non-$f_{\rm AG}$ frequency components, an ideal filter is used (Fig. 1), which exhibits zero impedance at the frequency $f = f_{\rm AG}$ and infinite impedance at the frequencies $f \neq f_{\rm AG}$. The load-circuit elements are then calculated/optimized through HB so as to fulfill the nonperturbation condition $Y_o = 0$, with Y_o being the complex ratio between the first harmonic component of the current through the AG and AG voltage. The fixing of the oscillation frequency through $f_{\rm AG} = f_o$ during the optimization prevents any frequency shift of the steady-state oscillation due to nonlinear effects.

The values $V_o = 1$ V (at the drain terminal) and $f_o = 4.5$ GHz have been used here for a varactor bias voltage $V_{\rm var} = -4.3$ V in the middle of the capacitance-variation range. The load-circuit elements are obtained through optimization with the goal $Y_o = 0$. Once the condition is achieved, the stability of resulting steady-state oscillation must be checked [6] together with the fulfillment of the conditions for the oscillation startup. The resulting design will be corrected so as to increase its frequency-division capabilities, according to the technique that is explained below.

In the analog divider by N, sensitivity to the input-generator signal and synchronization is achieved through the mixing of the input signal at $f_{\rm in}$ with the feedback signal at $(N-1)f_o$, which gives rise to a lower intermodulation product in the order of the oscillation frequency. Thus, the input circuit in Fig. 1 must behave as a bandpass filter at the generator frequency $f_{\rm in}$. After synchronization, the relationship $f_o = f_{\rm in}/N$ is fulfilled. In the design carried out here, the drain–current nonlinearity of the MESFET transistor mixes the two signals at $f_{\rm in}$ and $(N-1)f_o$ entering the gate port. Taking this into account, the above free-running oscillator design will be corrected so as to increase the harmonic amplitude of the self-oscillation at the orders $N-1=3$ (for the divider by $N=4$) and $N-1=4$ (for the divider by $N=5$) at the gate port. Although the design of the feedback network is essential, for the sake of simplicity, this network is made up here by the varactor diode only, with its complete equivalent model. The increase in the harmonic content will be achieved through modification of the operation point of the transistor, varying the bias sources and the load elements.

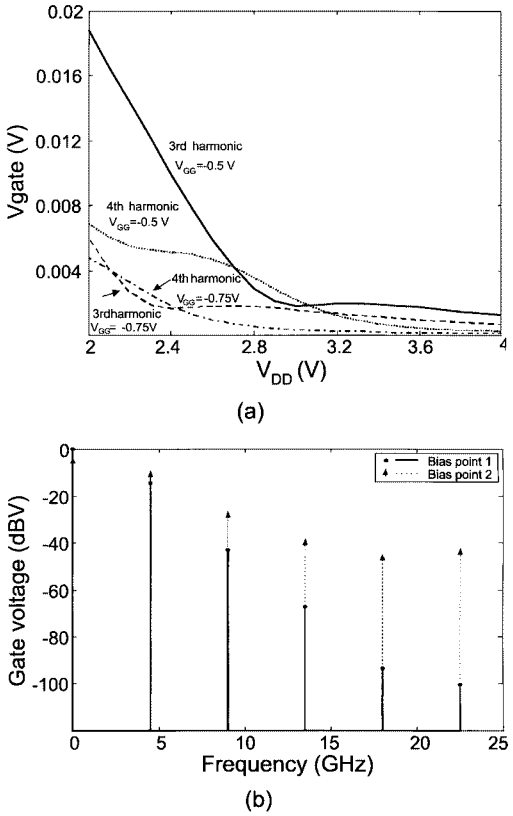

Fig. 2. Free-running oscillator. Technique for increasing the gate voltage amplitude at the harmonic orders $N = 3$ and $N = 4$, while keeping constant the oscillation frequency at $f_o = 4.5$ GHz. (a) A sweep is performed in the drain bias voltage $V_{\rm DD}$ for two values of the gate bias voltage $V_{\rm GG}$. Each point of the curves corresponds to a different design (different values of the oscillator load elements). (b) Comparison of the voltage spectrum at the gate terminal for two different designs with the same oscillation frequency.

To evaluate the harmonic amplitude at $(N-1)f_o$, a continuation technique is applied using the design seen above as the starting point. This allows the circuit oscillation at the desired frequency f_o to be maintained during the whole process. Different gate bias values $V_{\rm GG}$ between -0.5 and -1.5 V have been tested, performing a sweep in the drain bias $V_{\rm DD}$. The AG (at f_o, V_o) fixes, for each $V_{\rm GG}$, $V_{\rm DD}$, the desired value of the free-running oscillation frequency f_o and the voltage amplitude at the AG position. For each point of the $V_{\rm DD}$ sweep, the values of two circuit elements are determined so as to fulfill the nonperturbation conditions $Y_o(\gamma_1, \gamma_2) = 0$. To avoid convergence problems, a continuation technique is applied, using the final values γ_{1n-1}, γ_{2n-1} obtained for $V_{\rm DDn-1}$ as the initial guess for $V_{\rm DDn}$. The optimized parameters γ_1, γ_2 were the load resistance and inductance, obtaining the results of Fig. 2(a). The output power varies with $V_{\rm DD}$ and the load elements. However, the fixed AG amplitude avoids a severe decrease of the first harmonic amplitude during the process. As expected, the highest harmonic amplitudes correspond to corners of the characteristic curves with very nonlinear behavior. Of course, this is only a numerical analysis of the harmonic-generation capabilities of the oscillator topology so, once an operation point is selected, the oscillation startup conditions and the stability of the steady-state oscillation must be checked [6]. The analysis also allows the evaluation of the efficiency for different bias voltages and load-element values. The lowest efficiency corresponds to the highest harmonic values, thus, whenever this efficiency is a design constraint, a compromise must be achieved.

Two spectra, at the gate port, can be compared in Fig. 2(b). Both of them have exactly the same fundamental frequency ($f_o = 4.5$ GHz) and voltage amplitude ($V_o = 1$ V) at the AG position. Bias-point 1 is $V_{\rm GG} = -1$ V, $V_{\rm DD} = 4$ V, whereas bias-point 2, with the richest harmonic content, is $V_{\rm GG} = -0.62$ V, $V_{\rm DD} = 2$ V. The high harmonic content is filtered out at the circuit load, through the use of an inductive element. This capability to set the free-running oscillation frequency and voltage level, while increasing the harmonic content at the mixing port, constitutes the novelty of the analysis. For the final transistor bias values, the oscillation-frequency range versus the varactor bias voltage is $\Delta f_o = 1$ GHz, centered about $f_o = 4.5$ GHz.

III. Nonlinear Analysis of the Harmonic-Injection Frequency Divider

In this section, two different techniques for the analysis of harmonic-injection dividers are presented. The first technique is a semianalytical calculation that relies on the nonlinear analysis of the free-running oscillation (in the absence of RF input power) and the derivatives of the AG admittance function $Y(V_s, \omega_s, E_{\rm in})$ at the oscillation point. The second technique is a continuation algorithm of very simple application to HB software.

A. Semianalytical Estimation of the Synchronization Bands

When an input generator is connected to the oscillator circuit, the synchronization bandwidths, for small amplitude of this generator, can be approximately determined through a linearization of the circuit about its nonlinear free-running oscillator regime [9]. Actually, for small amplitude of the input generator, the synchronized solution can be treated as a perturbation of the free-running oscillation. Different estimations for the synchronization bandwidths have been provided in the literature [3], [9]. They enable a fast evaluation of the circuit capabilities as a frequency divider and allow design criteria to be obtained. However, in these expressions, only the first harmonic component of the free-running oscillation (at a given oscillation port) is taken into account. Moreover, the expressions depend on the quality factor of the embedding circuit, which is not accurate when both the real and imaginary parts of the total admittance/impedance (at the oscillation port) are functions of the oscillation amplitude and frequency. In order to clarify this, a new expression, only depending on the free-running oscillation and amplitude of the input generator, is derived in the following. The expression takes advantage of the AG that is used for the determination of the free-running oscillation [see Fig. 3(a)] and takes into account the entire harmonic content of this regime.

Let the free-running oscillation with fundamental frequency ω_o be considered. Provided that the amplitude of the first harmonic component of the voltage at a given circuit node n is V_o, a voltage AG, operating at $\omega_{\rm AG} = \omega_o$, with amplitude $V_{\rm AG} = V_o$, can be connected in parallel at the particular node n without perturbation of the steady-state solution [see Fig. 3(a)]. Now, an

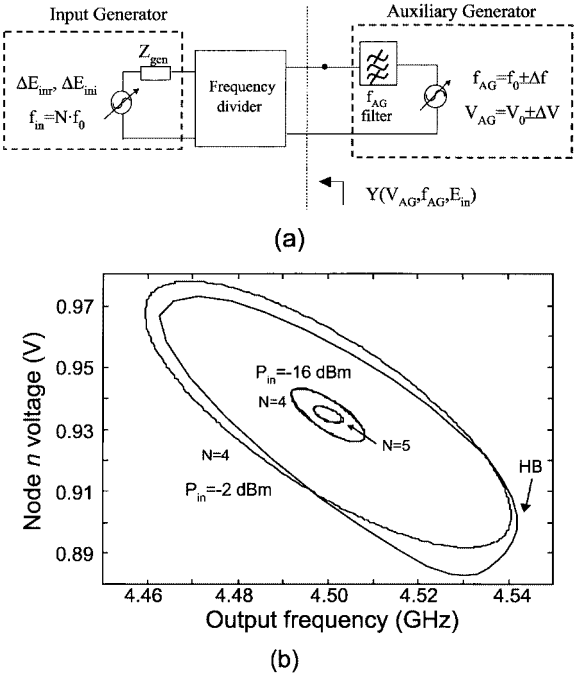

Fig. 3. Semianalytical estimation of the frequency-division bands of the harmonic-injection divider from the knowledge of the free-running oscillation solution and its derivatives. (a) Circuit arrangement, based on the use of an AG, to obtain the derivatives. (b) Comparison between the synchronization curves obtained from (2) and those obtained from HB, with 15 harmonic components. As the input power increases, less agreement is obtained due to the reduced validity of the linearization (2).

input RF generator $e_{\rm in}(t)$ will be introduced at any circuit location. Assuming a frequency division by N, the fundamental frequency and first harmonic component of the voltage at the node n will be, respectively, denoted $\omega_S \equiv \omega_{\rm in}/N$ and V_s. The input generator can then be expressed as $e_{\rm in}(t) = {\rm Re}(E_{\rm in}e^{j(\omega_{\rm in}+\phi)t})$ with ϕ being the opposite of phase shift between the frequency component at ω_s at the node n and the input generator at $N\omega_s$. In the presence of the AG, absolute dependence can be considered of the circuit variables on the amplitude and frequency of this generator [2], [4]. This enables writing

$$Y(V_s, \omega_s, E_{\rm in}e^{j\phi})V_s e^{j0} = 0 \tag{1}$$

where Y is the total current-to-voltage relationship at the fundamental frequency ω_s at the node n. For small input-generator amplitude $E_{\rm in}$, a Taylor-series expansion of (1), about the free-running oscillation point $(V_o, \omega_o, E_{\rm in} = 0)$ can be carried out as follows:

$$\frac{\partial Y_o}{\partial V_o}\Delta V_s + \frac{\partial Y_o}{\partial \omega_o}\Delta\omega_s = -\frac{\partial Y_o}{\partial E_{\rm inr}}E_{\rm in}\cos\phi - \frac{\partial Y_o}{\partial E_{\rm ini}}E_{\rm in}\sin\phi \tag{2}$$

with $\Delta\omega_s = \omega_s - \omega_o$ and $\Delta V_s = V_s - V_o$. Using the AG introduced at the node n, the derivatives of the free-running oscillation can be numerically calculated through increments in the frequency and amplitude of this generator [see Fig. 3(a)] with the HB equations as the inner tier. The use of the AG for this derivative calculation enables taking into account the entire harmonic content due to the absolute dependence of (1) on the AG value. The solution of (2) is an ellipse in the plane defined by ω_s and V_s centered about the free-running oscillation point ω_o, V_o. The inclination is determined by the derivatives of Y_o. The ellipse constitutes the synchronized solution curve for low-input generator amplitudes (due to the first-order expansion of the Taylor series). The infinite-slope points of the ellipse (one at each side) are local/global saddle-node bifurcations (see the Appendix). Thus, only one section of the synchronization curve (either the upper or lower section) can be stable.

The division bandwidth $\Delta\omega_{1/N}$ by the order N is given by twice the maximum value of the increment $\Delta\omega_s$ in (2) versus the phase shift ϕ as follows:

$$\begin{aligned}\Delta\omega_{1/N} &\equiv 2\left|\Delta\omega_s\right|_{\max} \\ &= 2E_{\rm in}\frac{\left|\left|\frac{\partial Y_o}{\partial E_{\rm inr}}\right|\sin\alpha\cos\phi_o + \left|\frac{\partial Y_o}{\partial E_{\rm ini}}\right|\sin\beta\sin\phi_o\right|}{\left|\frac{\partial Y_o}{\partial \omega_o}\right||\sin(\gamma)|} \\ \phi_o &= {\rm arctg}\left(\frac{\left|\frac{\partial Y_o}{\partial E_{\rm ini}}\right|\sin\beta}{\left|\frac{\partial Y_o}{\partial E_{\rm inr}}\right|\cos\alpha}\right)\end{aligned} \tag{3}$$

where α, β, and γ, respectively, are the angles, at the origin of the admittance diagram (free-running oscillation), between the derivatives $\partial Y_o/\partial V_o$ and $\partial Y_o/\partial E_{\rm inr}$ (in this order), between the derivatives $\partial Y_o/\partial V_o$ and $\partial Y_o/\partial E_{\rm ini}$, and between the derivatives $\partial Y_o/\partial V_o$ and $\partial Y_o/\partial\omega_o$. The dependence on the different angles prevents the establishment of a general criterion for the enlargement of synchronization bands. However, the cases $\alpha = \pm\pi/2$ and $\beta = \pm\pi/2$ are favorable since they increase the sensitivity of Y_o to the input generator. In addition, the magnitude of the frequency derivative $\partial Y_o/\partial\omega_o$ should be minimized.

Since the Y_o derivatives with respect to the free-running oscillation amplitude and frequency are independent of the division order N, the division capabilities for given N are determined by the sensitivity of Y_o to the input generator at $N\omega_s$. Expression (2) enables a simple evaluation of these capabilities. Here, it has been used for the prediction of the divided solutions at $N = 4$ and $N = 5$. The results are shown in Fig. 3(b), where they can be compared with those from the HB analysis through the technique explained in Section III-B using 15 harmonic components. For $P_{\rm in} = -16$ dBm, the division curves, both for $N = 4$ and $N = 5$, are almost overlapped with those from HB analysis. As the input power increases, the nonlinear behavior reduces the accuracy of the first-order Taylor-series expansion (2). This is why less agreement is obtained for $P_{\rm in} = -2$ dBm. To our knowledge, this is the first time that accurate expressions for the semianalytical calculation of frequency-division bands (only involving the knowledge of the free-running oscillation solution and its derivatives) are provided and demonstrated.

B. HB Analysis of Synchronization Bands

When the input-generator amplitude is not limited to small values, the frequency-divided solution by order N is obtained through HB simulation, using the AG, which now operates at the divided frequency $\omega_{\rm AG} = \omega_s = \omega_{\rm in}/N$ [2]. The AG amplitude $V_{\rm AG}$ and phase $\phi_{\rm AG}$ are either optimized or calculated (through an error-minimization algorithm) to fulfill the nonperturbation

condition $Y = 0$. If the variation of a parameter is now considered (for instance, the input frequency $\omega_{\rm in}$), the turning points of the ellipsoidal curves can be circumvented through parameter switching [2]. A simpler procedure is employed here, enabling better accuracy and more efficient simulation for divisions of high order. In the new procedure, a sweep is carried out in the AG phase $\phi_{\rm AG}$ between $\phi_{\rm AGo}$ and $\phi_{\rm AGo} + 2\pi/N$ calculating, for each point of the sweep, the two variables $V_{\rm AG}$ and the parameter in order to fulfill $Y = 0$. Another possibility is to set $\phi_{\rm AG} = 0$ and perform a $(0, 2\pi]$ sweep in the generator phase $\phi_{\rm in}$. Note that the circuit variables and the parameter ω_S are periodic in phase, as can be gathered from (2), and do not exhibit turning points versus this variable. This enables a straightforward tracing of the synchronization curve.

The technique has been applied to obtain the divided-by-four and divided-by-five solutions for the two input-power values $P_{\rm in} = -16$ dBm and $P_{\rm in} = -2$ dBm [see Fig. 3(b)]. Each solution point of the phase sweep is a point of the closed synchronization curve (see the Appendix). The synchronization bandwidth is given by the absolute minimum and maximum of the curve $\omega_{\rm in}(\phi_{\rm AG})$, i.e., $d\omega_{\rm in}/d\phi_{\rm AG} = 0$. A complementary stability analysis is necessary to determine the stable-solution section. In this case, the upper part of each curve (between the two outer turning points) is stable.

IV. Optimized Design of the Harmonic-Injection Divider

In this section, simulation tools are used for the correction of the frequency-divider design, when parasitic elements are taken into account. The external low-frequency feedback loop is introduced to increase the division bandwidth. A new technique based on the tracing of the synchronization locus on a two-parameter plane allows the optimum selection of the loop parameters.

A. Effect of the Parasitic Elements

In the analysis carried out here, the accuracy in the description of the linear network has been increased in successive steps with a gradual introduction of parasitic elements and microstrip discontinuities. Two major negative effects can be expected: the frequency shift of the synchronization bands and the reduction of these bands. The frequency shift in the synchronization band can be avoided through reoptimization of the free-running oscillation regime by setting the frequency of the AG to $\omega_{\rm AG} = \omega_{\rm in}/N$. This allows the free-running oscillation frequency and amplitude to be maintained at the desired values $\omega_o = \omega_{\rm in}/N$ and V_o. After each new inclusion of parasitic elements or discontinuity models, a couple of variables (for instance, a line length and width) are optimized/calculated so as to fulfill the free-running oscillation condition $Y_o = 0$. Setting the free-running oscillation frequency to ω_o ensures that the synchronization bands will be centered about this value, at least for small input power. The stability of the design, together with the oscillation startup conditions, must be checked at each step. After each free-running oscillation analysis, the synchronization band is determined. This technique enables the identification of any possible elements causing a substantial bandwidth reduction.

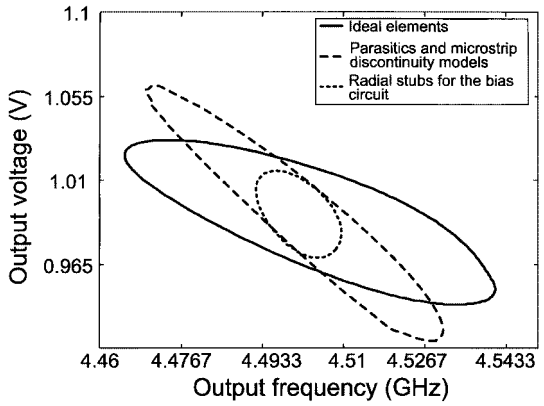

Fig. 4. Method to prevent the frequency shift of the division bands as parasitics elements and discontinuities are introduced in the circuit description during the design process. The solution curves, corresponding to the division order $N = 4$, have been obtained through HB with 15 harmonic components. The curves are always centered about the output frequency $f_s = 4.5$ GHz. The input power is, in all cases, $P_{\rm in} = -2$ dBm.

An example of the application of the technique is shown in Fig. 4. The synchronization curves corresponding to the division order $N = 4$ and input power $P_{\rm in} = -2$ dBm are shown at different stages of the circuit design. Note that all curves, obtained through HB, are centered about the values $f_o = 4.5$ GHz and $V_o = 1$ V as a result of the free-running optimization of the oscillator. The biasing networks have been implemented using radial stubs along with quarter-wave lines. The major reduction of the synchronization band has been found to be due to the input radial stub. After noting this, a different implementation of the bias filter should have been employed. However, the purpose of this study was the development of analysis and optimization tools only and no investigation of the optimum divider topology or implementation has been attempted. The demonstrator has been implemented on plastic substrate (Cuclad 2.17) using specific microwave drilling tools instead of chemical processes, in order to match the physical dimensions of the lines. Some notch filters to eliminate spurious responses have been used. Metallic via-holes have been used to minimize the parasitic inductance in ground connections.

B. Increase of Synchronization Bands Through an External Low-Frequency Feedback Loop

The injection-locking phase-locking techniques [3] rely on the addition of a low-frequency feedback loop to the injection-locked oscillator. Here, they are applied to the frequency divider by order N. The addition of the low-frequency feedback loop allows the use the low-frequency intermodulation term $|f_{\rm in} - Nf_o|$ provided by the $i_{\rm DS}(v_{\rm GS})$ nonlinearity to increase the sensitivity to the input generator and, thus, the synchronization bands. The term gives rise to a low-frequency error signal $v_D(t)$ at the transistor drain terminal. This signal is extracted through a choke and amplified in the feedback loop. The differential amplifier compares the low frequency-signal extracted at the drain voltage with a dc reference voltage. The amplifier output is connected to the varactor diode and this modifies the self-oscillation frequency so as to decrease

the frequency error, as in a phase-locked oscillator. Thus, phase-locking techniques and harmonic injection are combined to increase the frequency-division bands. The enlargement of the synchronization bandwidth depends on the voltage gain G_a of the dc amplifier and the phase shift that this amplifier introduces in the low-frequency feedback signal [3]. Here, the output of the feedback loop is connected to the cathode of the varactor diode. For each phase shift ϕ, the new value of the divided frequency ω_s' can be approximated as follows:

$$\omega_s' = \omega_o + kG_aV_d\cos(\phi) + \Delta\omega_s(\phi) \tag{4}$$

where $\Delta\omega_s(\phi)$ is given by (2) and k is the frequency sensitivity of the VCO. Thus, the new synchronization bandwidth can be determined calculating the maximum of (4) with respect to ϕ through derivation. However, the introduction of the loop filter modifies the derivatives of Y_o in (2). In addition, the combination of (4) and (2) only applies when the loop bandwidth equals or exceeds the locking bandwidth [3]. Instead, a more accurate prediction, for low input-generator power, can be obtained recalculating the Y_o derivatives in the presence of the loop and applying (2). It must be taken into account that the synchronized solutions in the harmonic-injection divider with the low-frequency feedback loop are expressible through a one-fundamental Fourier-series expansion of the circuit variables. Thus, frequency-domain analysis techniques, such as the linear estimation (2) or HB must be able to provide these solutions.

C. Synchronization Loci Versus Two Parameters

In practical circuits, it can be of primary interest to predict the influence of a given parameter η (such as the input generator amplitude) over the frequency bandwidth of synchronized behavior. When this second parameter η is taken into consideration (in addition to $\omega_{\rm in}$), the nonlinear evolution of the synchronization bands can be analyzed through HB by performing two nested sweeps. In the external sweep, the second parameter η is varied in the expected range. In the case of the input generator amplitude $E_{\rm in}$, for instance, this range is between small signal and a few volts. In the internal sweep, the input-generator phase $\phi_{\rm in}$ is varied between 0° and 360°, while keeping $\phi_{\rm AG} = 0$. Thus, double sweep, in η and $\phi_{\rm in}$ is carried out. At each point of the double sweep, the AG frequency $\omega_{\rm AG}$ and amplitude $V_{\rm AG}$ are determined. Since the phase variation is always limited to the interval $[0°, 360°]$, the double sweep does not require a big computational effort.

The double sweep provides conic figures in the three-dimensional space defined by $\omega_{\rm in}$, η, and $V_{\rm AG}$. If the synchronization curves are regular enough, the synchronization locus in the plane $\omega_{\rm in}$, η is simply given by the projection of the three-dimensional figure over this plane (see the Appendix). If the synchronization curves contain more than two turning points (one at each side), a projection of each of these points is necessary to take into account the possible hysteresis phenomenon [2], [4]. This technique enables tracing the bifurcation loci in a very simple fashion (through two nested sweeps). Alternatively, when using in-house software, the locus can be obtained from the turning-point condition $d\omega_{\rm in}/d\phi_{\rm in}(\phi_{\rm in}, \eta) = 0$, which provides a curve in the plane $\omega_{\rm in}$, η.

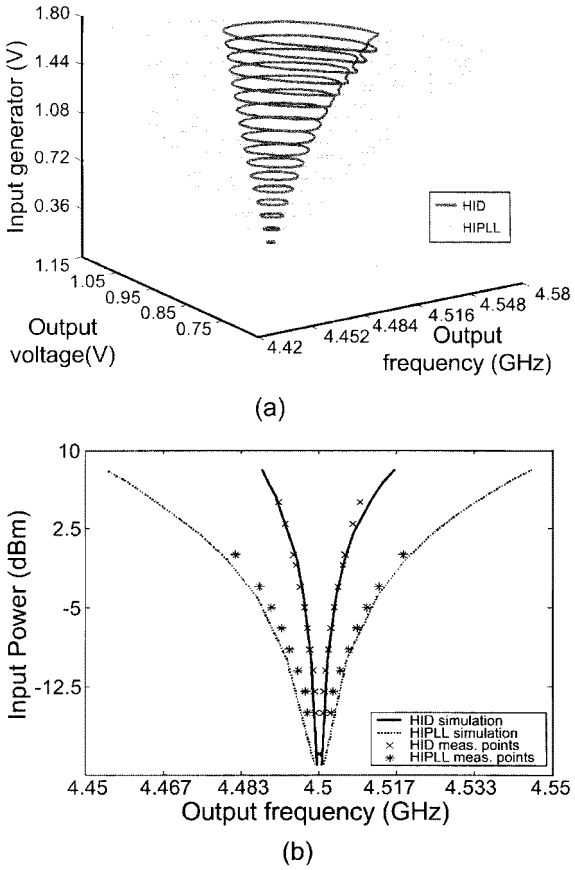

Fig. 5. Frequency divider by $N = 4$ for the bias point $V_{\rm GG} = -0.5$ V and $V_{\rm DD} = 2.2$ V. "HIPLL" stands for harmonic-injection phase-locked loop and "HID" stands for harmonic-injection divider. (a) Solution curves in the three-dimensional space, defined by the input-generator amplitude, divided by four frequency f_s and output voltage. (b) Projection over the plane defined by the input-power and output frequency f_s, showing the evolution of the operation bands versus the input power.

The above technique has been applied to obtain the variation of the frequency-division bands of the divider circuit, with and without the inclusion of the low-frequency feedback loop, versus the input power. The voltage gain of the low-frequency amplifier is $G_a = 20$ dB. The two conic figures for $N = 4$ are represented in Fig. 5(a), whereas the projection of both figures over the plane defined by the output frequency and input power (f_s, $P_{\rm in}$), giving the two synchronization loci, is shown in Fig. 5(b). For the input-power values that have been employed here, the self-oscillation is not extinguished so the two bifurcation loci are open in the upper part. As can be seen, the introduction of the feedback loop enables a three-times larger synchronization bandwidth for the higher input-power values. Measurement points have been superimposed with very good agreement.

The projection over the plane defined by the output frequency and output power (f_s, $P_{\rm out}$) is shown in Fig. 6. Note the similar inclination of the two families of solution curves (with and without feedback loop). Smooth variations of output power versus the divided frequency are obtained for all the input-power values. The upper section of each synchronization curve (defined between the two turning points) is stable, as has been verified through the systematic application of the

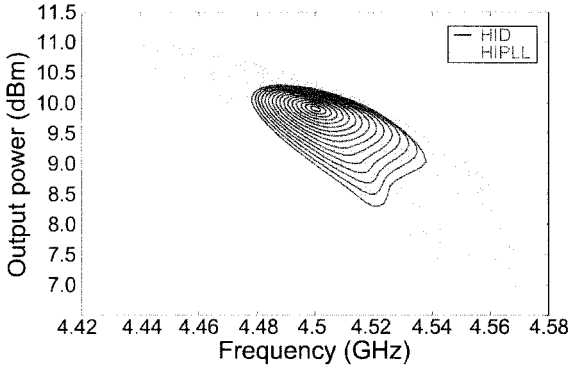

Fig. 6. Output power for $N = 4$ versus the divided frequency f_s for different levels of input power with (HIPLL) and without (HID) an external feedback loop.

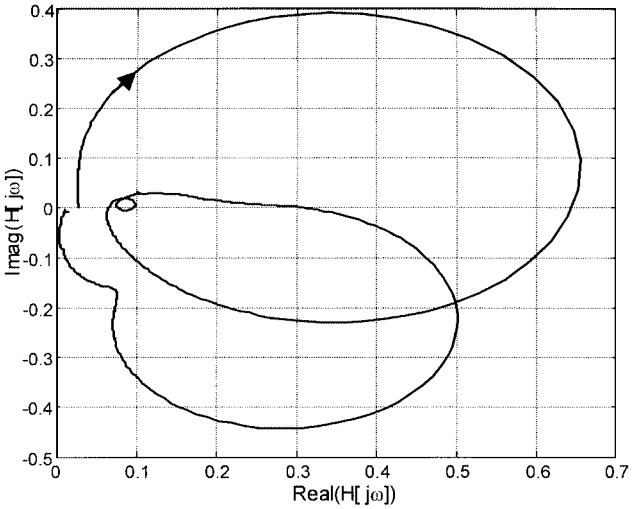

Fig. 7. Stability analysis of a solution point of the frequency divider by $N = 4$ with the low-frequency feedback loop. For this particular plot, the input frequency is $f_{\rm in} = 18$ GHz and the input power is $P_{\rm in} = -10$ dBm. The systematic application of this tool has shown the stability of the upper sections of the solution curves in Fig. 6.

Nyquist stability criterion [6]. The stable plot resulting from one of these analyses, corresponding to the input frequency $f_{\rm in} = 18$ GHz and the input power $P_{\rm in} = -10$ dBm, is shown in Fig. 7. Due to the closed shape of the solution curves and the stability of the entire upper sections of these curves, the observation of hysteresis would be unlikely. This absence of hysteresis has been confirmed experimentally.

The variations of the frequency-division bandwidth versus the loop-amplifier gain have also been analyzed. The synchronization locus (Fig. 8) has been traced in the plane defined by the output frequency $f_s = f_{\rm in}/4$ and the voltage gain G_a, for constant input power $P_{\rm in} = -2$ dBm. The locus shows that larger synchronization bandwidths can be obtained for higher values of the amplifier gain. To our knowledge, this is the first time that this synchronization analysis is applied to frequency dividers by $N = 4$ and to frequency dividers with external feedback loop.

The conic figures corresponding to the division order $N = 5$ are shown in Fig. 9. Fortunately, the visible turning points in the middle of the division bands take place in the lower unstable sections of the curves and do not give rise to hysteresis. For input

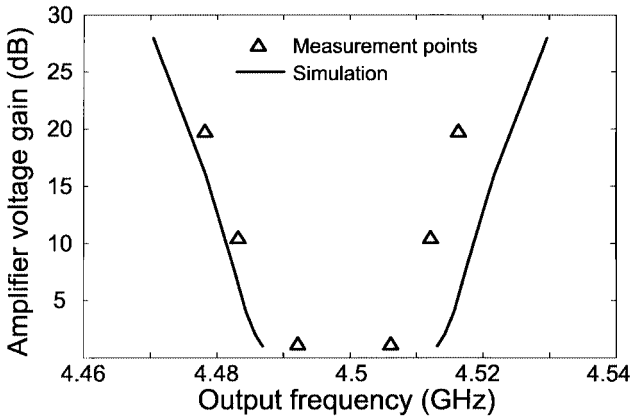

Fig. 8. Variations of the frequency division band for $N = 4$ with the voltage gain G_a of the loop amplifier for the input-power value $P_{\rm in} = -2$ dBm. The two curves constitute the saddle-node bifurcation loci of the divider circuit in the plane defined by the output frequency f_s and G_a.

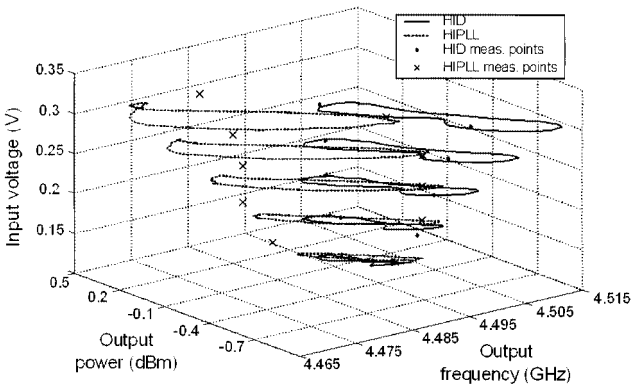

Fig. 9. Synchronization curves of the divider circuit, when operating as frequency divider by $N = 5$, in the three-dimensional space defined by the divided frequency, input-generator voltage, and output voltage.

frequency $f_{\rm in} = 18$ GHz, the relatively large oscillation bandwidth of the varactor-controlled oscillator enables the switching of the division order between $N = 4$ and $N = 5$. For $N = 5$, the central frequency of the divider must be switched (through the varactor bias) to $f_o = 3.6$ GHz. For $V_{\rm var} = 0$ V, the division order is $N = 4$, whereas for $V_{\rm var} = -13$ V, this order is $N = 5$. The experimental spectra are shown in Fig. 10. Additional filtering of the divided frequency might be necessary for some applications.

V. Ultrasubharmonic Synchronization

The possibility of ultra-subharmonic synchronization in the MESFET-based divider has been investigated. The use of fractional-order dividers in a transmitter–receiver system would enable reducing the number of synthesized oscillators since the output of one synthesizer at ω_1 could be used to synchronize a VCO at $\omega_2 = M/N\omega_1$. The synchronization bandwidth decreases with M and N and may be negligible for most M and N values (see the Appendix). However, at least for relatively small values of M and N, this kind of synchronization can be practically achieved.

The prediction through simulation of fractional synchronization bands is difficult. In an earlier work [10], these bands were

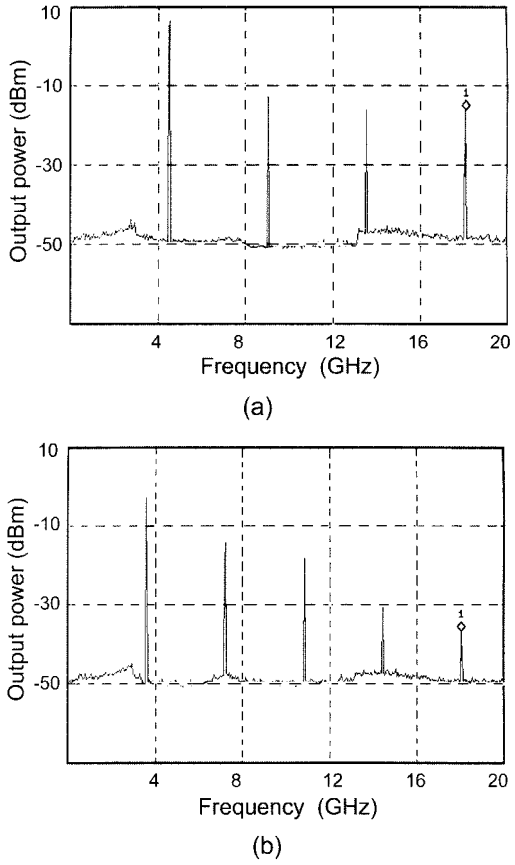

Fig. 10. Experimental switching of the division order of the frequency divider through the modification of the bias voltage of the varactor diode. (a) Bias voltage $V_{\rm var} = 0$ V. The division order is $N = 4$. (b) Bias voltage $V_{\rm var} = -13$ V. The division order is $N = 5$.

estimated through admittance diagrams, obtained by sweeping the phase of an AG. Here, the new technique (in which the amplitude and phase of the solution curves are calculated versus the AG phase) is employed. The synchronization band at M/N ($M \neq 1$) is analyzed using a Fourier-series expansion at the fundamental frequency $\omega_f = \omega_s/N$. Thus, the oscillation frequency is $\omega_s = N\omega_f$, while the input generator operates at $\omega_{\rm in} = M\omega_f$. The frequency ω_f is due to intermodulation between $\omega_{\rm in} = M\omega_f$ and $\omega_s = N\omega_f$. The use of an AG at the oscillation frequency $N\omega_f$ enables the tracing of the synchronization curves through a phase sweep.

The synchronized solution corresponding to the rotation number $M/N = 2/3$ has been analyzed here. The closed solution curve, versus the input frequency, has been calculated before and after the introduction of the low-frequency feedback loop (Fig. 11). The simulation results can be compared, in each case, with the two experimental points showing the beginning and end of the synchronization band. For the relatively high input-generator power, the bending of the respective Arnold tongue gives rise to solution curves that are not centered about the free-running oscillation frequency. To our knowledge, this is the first time that these division bands of fractional order have been obtained through frequency-domain simulation. The enlargement of the bands through the low-frequency feedback loop enables the use of this kind of synchronization in practical communication systems.

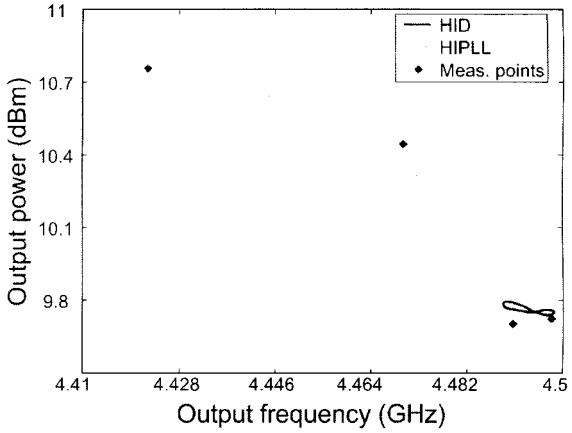

Fig. 11. Frequency division by the fractional order $N = 2/3$ with external feedback loop. For the relatively high input-generator power, the bending of the synchronization locus gives rise to solution curves that are not centered about the free-running oscillation frequency.

VI. Phase-Noise Analysis

For the phase-noise analysis of the frequency divider, the conversion-matrix approach [11], [12] has been employed. This avoids the need of obtaining a system equivalent of the circuit, identifying the different system blocks, as has been done in [3]. The circuit is analyzed as a whole, with noise generators, modeling the noise contributions. A set of noise sources operating at the sidebands $k\omega_o + \Omega$ is considered with $-NH \leq k \leq NH$ and $0 \leq \Omega \leq \omega_o$ being the frequency offset from the carrier. The noise-generator vector at the sideband $k\omega_o + \Omega$ is denoted $\overline{N}_k(\Omega)$. The noise perturbations give rise to sidebands $p\omega_o + \Omega$ with $-NH \leq p \leq NH$ in the circuit variables. For their calculation, the HB equations are linearized about the nonlinear steady state, replacing the nonlinear devices by their conversion matrixes and obtaining the linear-network matrixes at the sidebands. The sideband phasor of the output voltage at the load resistance at $p\omega_o + \Omega$ is given by

$$\Delta V_p(\Omega) = \sum_{k=-NH}^{NH} M_{pk}(\Omega)\overline{N}_k(\Omega) \tag{5}$$

with M_{pk} being conversion matrixes. The correlation coefficients of the output voltage are given by $\langle \Delta V_p \Delta V_r^* \rangle$. In this calculation, the correlation matrices of the noise-source bands must be taken into account.

In the analysis carried out here of the frequency divider by $N = 4$, the noisy input generator is represented by an ideal source at $\omega_{\rm in} = 4\omega_s$ and two noise sidebands at $\Omega \pm 4\omega_s$. The AM noise of the input generator is neglected for the calculation. For the oscillator contributions, a voltage noise source, in series with the transistor gate, is introduced, to account for the low-frequency noise, together with white noise sources. Typical values have been used, with experimental fitting. In Fig. 12, the phase-noise spectral density of the divider has been evaluated for $f_{\rm in} = 17.8$ GHz and $P_{\rm in} = -10$ dBm before and after the introduction of the feedback loop, and compared with the phase noise of the input source and the phase noise of the free-running oscillator. The latter has been calculated using both the carrier-modulation approach [11] (for small frequency offsets) and

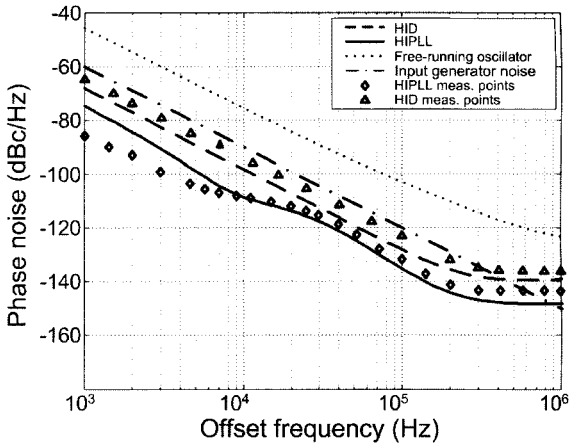

Fig. 12. Phase-noise spectral density of the frequency divider by $N = 4$ for $f_{\rm in} = 17.8$ GHz and $P_{\rm in} = -10$ dBm.

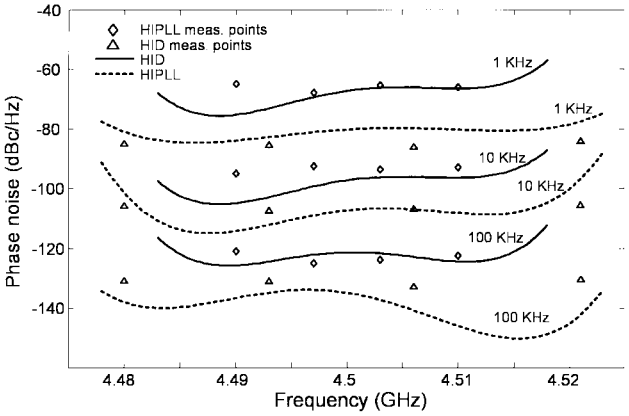

Fig. 13. Variations of the phase-noise of the frequency divider with and without low-frequency feedback loop, along the division band, for constant input power $P_{\rm in} = -10$ dBm and different values of the frequency offset from the carrier. In all cases, an increase is observed at the limits of the division band.

the conversion-matrix approach. The experimental phase-noise spectra, for the divider without low-frequency loop and for the divider with low-frequency loop, are also shown. Near the carrier, the output of the harmonic-injection divider shows a phase-noise improvement of approximately 9 dB close to the theoretical 12 dB of static predictions. The introduction of the low-frequency feedback loop gives rise to an improvement of approximately 17 dB. The slight disagreement close to the carrier is believed to be due to inaccuracy in the model of the loop amplifier. Far from the carrier, the two designs reach, as expected, the phase-noise level of the free-running oscillator.

The phase-noise reduction in the divider with low-frequency loop is due the high gain of the amplifier [3]. The phase-noise spectrum shows a "bump," related to the phase margin of the linearized divider, under the presence of the feedback loop. The bump is observed around the damped natural frequency of the system, which closely depends on the location of the loop-amplifier pole ($f = 35$ kHz), amplifier gain, and transistor operation point [3]. The simulation through the conversion matrix approach accurately predicts this bump.

Fig. 13 shows the variation of the phase-noise spectral density along the synchronization curve for constant input power $P_{\rm in} = -10$ dBm and different values of the offset frequency.

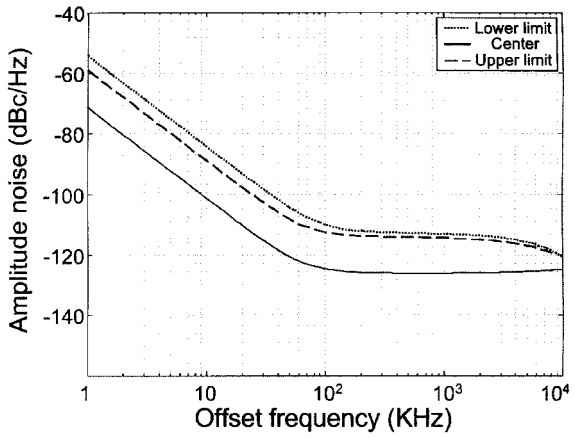

Fig. 14. Spectral density of the amplitude noise, for three different values of offset frequency, in the middle and at the two ends of the division band ($f_{\rm in1} = 17.932$ GHz and $f_{\rm in2} = 18.072$ GHz). The input power is $P_{\rm in} = -10$ dBm.

As can be seen, the phase noise increases as the limits of the synchronization band are approached, in agreement with the results of other authors [13]. Close to the saddle-node bifurcations that constitute the ends of the synchronization band, a Floquet multiplier of the periodic regime approaches the real value $m_i = 1$ [14]. A multiplier with magnitude close to one means a long-lasting transient due to the relationship between the Floquet multipliers and exponents $m_i = e^{(\sigma + {\rm j}k\omega_s)T_s}$, with T_s being the period of the steady-state regime and k being an integer. This slow transient, continuously interrupted by the noise perturbation, gives rise to noise amplification of the noise spectrum about f_s and its harmonic components [14]. This noise amplification will generally be unequal at the two sidebands of the output voltage. It is linear up to the immediate neighborhood of the bifurcation [15] so it can be predicted through the conversion-matrix approach (5). The noise amplification is in close relationship with the stability margin, which decreases as the borders of the ellipsoidal synchronization curve are approached.

The simulation of the amplitude noise in the divider without feedback loop for $P_{\rm in} = -10$ dBm in the middle and close to the two limits of the division band ($f_{\rm in1} = 17.932$ GHz and $f_{\rm in2} = 18.072$ GHz), is shown in Fig. 14. The impact of the critical multiplier on the noise spectrum depends on the way how this multiplier varies with the input frequency, i.e., $m_i(\omega_{\rm in})$, which gives rise to the asymmetry in the curves of Figs. 13 and 14. Note that the noise degradation occurs in the immediate neighborhood of the limits of the synchronization band so the divider is useful for most of the synchronization bandwidth.

VII. Conclusions

The design of analog frequency dividers relies on the multiple Arnold tongues of highly nonlinear oscillators and requires powerful simulation tools with control over the self-oscillation and its harmonic content. In this paper, design and optimization tools have been provided with new simulation techniques that efficiently circumvent the turning-point problem of the synchronization curves and the lack of accuracy in analog divisions by high order. The techniques enable setting the divider frequency and output power and overcome some of the undesired effects

of parasitic elements. Phase-locking techniques have also been employed, through the inclusion of a low-frequency feedback loop, to increase the division bands. The harmonic-injection phase-locked dividers are nonlinearly simulated and optimized. The output noise is analyzed through the conversion matrix approach. The variations of the phase and amplitude noise along the synchronization band have also been studied and related with the proximity to the saddle-node bifurcations, delimiting the synchronization bands. Using the new techniques, a harmonic-injection phase-locked divider by four and five, based on a MESFET transistor, has been designed and experimentally characterized, with very good results.

APPENDIX

Here, some concepts of nonlinear dynamics [4], [7] that directly apply to harmonic-injection dividers are summarized to help the understanding of this paper.

A. Phase-Space and Stability

In the phase-space representation of the solutions of a nonlinear circuit, a state variable x_i is assigned to each axis of the coordinate system [4]. In forced systems (with time-varying generators), the time must be included in the state-variable set. For a periodic forcing (as in a frequency divider), the phase of this generator can be used instead. In the phase space, the steady-state solutions give rise to bounded sets or limit sets. The stable solutions are attractive for all their neighboring trajectories and are called attractors. Solutions that are attractive only for some of their neighboring trajectories are unstable and will be called saddle-type solutions. Only stable solutions are physically observed. A periodic solution, with one independent fundamental, gives rise to a limit cycle in the phase space. A quasi-periodic solution, with two incommensurate fundamentals, gives rise to a limit torus.

B. Solutions of Harmonic-Injection Dividers

Harmonic-injection dividers exhibit a free-running oscillation in the absence of input signal. Let the frequency of this oscillation be ω_o (autonomous frequency). When the input generator, at the frequency $\omega_{\mathbf{in}}$ is connected, the autonomous frequency ω_o is influenced by this generator and it changes slightly from its free-running value. The rotation number [2], [4], [7] is defined $r = \omega_o/\omega_{\mathbf{in}}$. According to the rational or irrational value of r, there are two main types of steady-state solution. For an irrational rotation number, the frequencies $\omega_{\mathbf{in}}$ and ω_o are incommensurate and the circuit behaves as a self-oscillating mixer. The solution in the phase space is a two-dimensional torus, in agreement with the two individual rotations at $\omega_{\mathbf{in}}$ and ω_o. If variations in the input generator frequency or amplitude (circuit parameters) are now considered, the rotation number r may take a rational value that remains constant for some parameter intervals. For a rational value $r = 1/N$ or $r = M/N$, with $M < N$, the solution is periodic with period $NT_{\mathbf{in}}$. In the phase space, this solution gives rise to a cycle with period $NT_{\mathbf{in}}$.

C. Poincaré Map

The Poincaré map of a steady-state solution is obtained through the intersection of the corresponding limit set in the phase space, with a transversal surface. In case of a nonautonomous circuit, with a periodic input generator of period T, this intersection can be obtained by sampling the steady-state solution and integer multiples nT of the input generator period. This is equivalent to an intersection with the surface $\theta = 2\pi/Tt_o$ with an arbitrary time value t_o after the steady state has been achieved [4]. For an M/N solution, the period is NT and this intersection provides N fixed points. The invariant sets resulting from the application of the map to stable solutions are attractors of the map. A torus (or quasi-periodic solution) in the phase space gives rise to a closed curve in the Poincaré map, composed of discrete points that are eventually filled. Stable solutions or attractors in the phase space give rise to attractors in the Poincaré map.

D. Solution Curves Versus a Parameter

The solution path of a given nonlinear system is the set of solutions of the system that is obtained when a parameter is continuously varied. When using HB, the solution path can be traced in terms of the value of one of the harmonic components or, for instance, in terms of the output power. In the harmonic-injection frequency dividers, closed solution curves are obtained when traced versus the input frequency.

E. Bifurcations

A bifurcation is a qualitative variation of the stability properties of a solution, when a parameter is continuously modified. The local bifurcations are due to stability changes in a single steady-state solution. The global bifurcations are due to qualitative changes in the global configuration of the stable and unstable manifolds of a saddle-type solution [4]. In the harmonic-injection divider, the most relevant bifurcations are those delimiting the synchronization bands, i.e., providing, versus the parameter or parameters, the border between frequency-divider behavior (by a given order N) and self-oscillating mixer behavior. These bifurcations generally take place at the infinite slope points of the closed synchronization curves. They are saddle-node bifurcations of local/global type, at which loss of synchronization occurs.

F. Saddle-Node Bifurcations of Local/Global Type

Turning-point bifurcations occur at points of infinite slope of a solution curve, versus a given parameter. A turning (or fold) point of a solution curve, versus a circuit parameter, is a point with infinite slope. At this point, a system pole crosses the imaginary axis through zero, which gives rise to a singularity of the Jacobian matrix of the HB system and, thus, to the infinite slope. When the pole crosses the imaginary axis, a qualitative stability change takes place in the system. Thus, the turning point necessarily separates sections of the solution curve with different qualitative stability (different numbers of unstable poles). In some cases, the turning point separates a stable and an unstable section. Therefore, it can be viewed, in the Poincaré map, as a point of collision between a stable and saddle point. The two

types of solution are destroyed by the collision, which constitutes a saddle-node bifurcation. In a local saddle-node bifurcation, the solution evolves toward a different attractor after the bifurcation. In the local/global saddle-node bifurcation, prior to the bifurcation, the unstable manifold of the saddle forms a loop, containing the node [4], [7]. Only the node is physically observed. However, when the saddle-node bifurcation takes place, the loop gives rise to an invariant closed curve in the Poincaré map, i.e., to a quasi-periodic solution. This determines the loss of synchronization.

G. Bifurcation Loci

In the harmonic-injection divider, the input-generator power P_{in} is often considered as an analysis parameter, together with the input frequency f_{in}. In the plane defined by f_{in} (horizontal axis) and P_{in}, the set of saddle-node bifurcations delimiting the division bands by the order M/N is a V-shaped curve. This curve is the synchronization locus, also called the *Arnold tongue*. Synchronized solutions exist inside the tongue. There is a synchronization locus (or Arnold tongue) for each rotation number M/N. Theoretically, in between any two synchronization bands M_1/N_1 and M_2/N_2, there is another synchronization band $(M_1+M_2)/(N_1+N_2)$, which should give rise to infinite synchronization bands and, when represented versus the input frequency, to a fractal dimension figure, known as the *devil's staircase*. The synchronization bandwidth decreases, however, with M and N.

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